

Form PTO 1449
(Modified)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY DOCKET NO.
247943US-2XSERIAL NO.
10760,449

LIST OF REFERENCES CITED BY APPLICANT

APPLICANT

Tatsuya KUNIKIYO, et al.

FILING DATE
January 21, 2004

GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>MX</i>	AA	6,300,765	10/09/01	CHEN			
<i>MX</i>	AB	5,999,010	12/07/99	ARORA ET AL.			
	AC						
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	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	AO					
	AP					
	AQ					
	AR					
	AS					
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	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

<i>MX</i>	AW	Jai-Hoon SIM, et al., 1998 Symposium on VLSI Technology Digest of Technical Papers, Pages 32-33, "THE IMPACT OF ISOLATION PITCH SCALING ON V_{th} FLUCTUATION IN DRAM CELL TRANSISTORS DUE TO NEIGHBORING DRAIN/SOURCE ELECTRIC FIELD PENETRATION," June 9-11, 1998
<i>MX</i>	AX	James C. CHEN, et al., Technical Digest of IEDM, pages 69-72, "AN ON-CHIP, ATTOFARAD INTERCONNECT CHARGE-BASED CAPACITANCE MEASUREMENT (CBCM) TECHNIQUE," 1996
<i>MX</i>	AY	K. YAMADA, et al., 2003 Symposium on VLSI Technology Digest of Technical Papers, pages 111-112, "ACCURATE MODELING METHOD FOR DEEP SUB-MICRON Cu INTERCONNECT," June 10-12, 2003/Kyoto
	AZ	

☐ Additional References sheet(s) attachedExaminer *M. Kramsky*Date Considered *10/27/05*

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



LIST OF RELATED CASES

	<u>Docket Number</u>	<u>Serial or Patent Number</u>	<u>Filing or Issue Date</u>	<u>Inventor/ Applicant</u>
<i>MA</i>	PER CLIENT	10/355,068	01/31/03	YAMASHITA et al.
<i>MA</i>	227009US2X	10/232,689	09/03/02	KUNIKIYO et al.
<i>MA</i>	229544US2	10/287,537	11/05/02	OKAGAKI et al.
<i>MA</i>	247943US2X*	10/760,449	01/21/04	KUNIKIYO et al.